CLAIMS

1. A processing system for providing a distributed directory based coherence protocol utilizing an associated memory having a coherence directory and associated directory data, the associated memory further comprising:

a plurality of memory blocks each associated with different directory data;

a plurality of buffers interconnected to the memory;

a plurality of processing elements, each of the processing element coupled to different buffers of the plurality of buffers;

means for requesting selected the memory blocks from the memory;

means associated with the memory, responsive to the means for requesting for delivery, in response to the requesting, for delivery of a corresponding memory block of the memory blocks, a corresponding set of the coherence directory data from the memory, to an associated element of the processing elements; and

means for the processing elements for detecting the delivery of the memory block, if the memory block of the processing element is available for a particular access mode, and if not, performing coherence actions corresponding to the coherence directory data.

2. The system of Claim 1, wherein the memory blocks are configured to provide the system memory space.

3. The system of Claim 1, where the memory blocks are used to provide a level of cache in the system memory hierarchy.

4. The system of Claim 1, where the processing elements are connected with the buffers connected to the memory via point to point links.

5. The system of Claim 1, where at least one processing elements contains at least a first processor, and at least one processing elements contain at least a second processor.

6. The system of Claim 1, wherein the coherence is performed by the processing elements, said processing elements conveyed through said system via a physical coherence bus and a logical coherence bus, said busses further comprising:

multiple point-to-point linkages;

multiple point-to-point coherence ring;

unique signaling primitives, the unique signaling primitives signaling between nodes provided by the system; and

a messaging and signaling system provided in the memory.

7. The system of Claim 1 wherein the processor additionally comprises a microcode, a firmware, and a software code for processing said coherence.

8. The system of Claim 1 wherein memory requests resulting in coherence actions update directory information to at least one state not corresponding to an indication of one of resident, shared, and exclusive states.

9. The system of Claim 8 where processing elements causing such at least one state resolve them using protocol requests.

10. The system of Claim 9 where other processors detect the at least an on state and back off and retry at a later time, until the node having generated the at least one state, resolves the at least one state, by performing coherence actions and updating the coherence directory.

11. The system of Claim 1, wherein the memory supports access to directory information by performing a read, write, and at least one Boolean operation on directory information.

12. A method implementing a distributed directory based coherence protocol, comprising:

requesting a memory block from a memory hierarchy level having a coherence directory and associated directory data,

generating a response including memory data and coherence directory data and updating directory information,

receiving a response including memory data and coherence directory data from the memory hierarchy level,

a testing step to indicate whether received directory data is compatible with required access mode,

a step of performing coherence actions if the test indicates one of incompatibility or possible incompatibility; and,

a step of providing data to a requestor of memory data.

13. The method of Claim 12, wherein requests and responses are performed by sending and receiving data over logical point to point links.

14. The method of Claim 12, wherein the steps of generating a response and updating directory information are performed

atomically with respect to other generating and updating steps.

15. The method of Claim 12, wherein the directory information includes a state indicating that at least one node is performing coherence actions as a result of receiving the response.

16. The method of Claim 12, where the step of performing coherence actions uses additional directory information to efficiently perform the coherence actions.

17. The method of Claim 12, wherein coherence actions are performed by at least one processing element by sending coherence requests to other processing elements.

18. The method of Claim 17, wherein those other processing elements are identified by additional information provided in the coherence directory.

19. The method of Claim 12 wherein the response containing memory data and coherence directory data is transmitted in a single response.

20. The method of Claim 12 wherein a response contains multiple data and coherence directory entries.

21. The method of Claim 12 wherein the response is generated under the control of a tag array.

22. The method of Claim 12 wherein the update of directory information is limiting to setting or resetting a plurality of bits, in response to the requesting step.

23. An apparatus using a memory component as integration point for building a symmetric multiprocessing system, consisting of multiple processing elements, each processing element containing at least one processing unit.

24. The apparatus of Claim 23 wherein integration includes means for providing coherence using directory information in the memory and distributed directory management.

25. The apparatus of Claim 23 wherein coherence protocol implementation is based on processing elements reading, writing and updating directory information in the the memory.

26. The apparatus of Claim 25, wherein coherence actions are performed by using communication between processing elements.

27. The apparatus of Claim 23 wherein the memory component also serves as signaling integration point, the memory component being the conduit for all signaling between processing elements.

28. The apparatus of Claim 23 wherein the memory component serves as physical integration point for building a symmetric multiprocessing system.

29. A computer program product for authenticating code in a computer system, the computer program product having a medium with a computer program embodied thereon, the computer program comprising:

computer code for providing a distributed directory based coherence protocol incorporating buffer logic; and

computer code for ordering a memory block movement command having an associative coherence directory data movement command.

30. A directory-based coherence system with distributed directory management utilizing buffers for providing data coherence in a computer system, including a computer program comprising:

computer code for requesting memory blocks from memory through requesting, acknowledging and delivery logic; and

computer code for ordering a memory block movement along with computer code for having an associative coherence directory data movement command.